Guru Gobind Singh Indraprastha University
"A State University established by the Govt. Of NCT Delhi"
Sector 16-C, Dwarka, New Delhi – 110078

F. No.: GGSIPU/CCGPC/2023/ 1061 1st July 2024

Sub. Placement opportunity for B.Tech ECE students of USICT, GGSIP University of the batch passed out in year 2024 in the company "Sophrosyne Technologies"

Dear Placement Officer,

Greetings from CCGPC, GGSIPU!!!

Please find below details of Placement opportunity for B.Tech ECE students of USICT, GGSIP University of the batch passed out in year 2024 in the company "Sophrosyne Technologies" for your reference and circulation to students to apply on given link by **2nd July 2024:**

Registration Link – **https://forms.gle/KaZ1TBtphhF8vCA2A**

Name of Company – Sophrosyne Technologies

Roles –

1. Analog Circuit Design
2. Analog Layout Design
3. Digital circuit Design

Eligibility – Students of B.Tech ECE from USICT, passed out in 2024

CTC – INR 5.6 lacs per annum post completion of training period

Training period – 5 months classroom training followed by 3 months on job training (OJT) through live projects

Stipend During Training – Stipend will be INR 20,000 per month plus some special allowances

Job Location – Manipal, Karnataka

Selection Procedure:

1. Written Test: Aptitude and basic knowledge of electrical/electronics engineering.
2. Interview: Candidates who excel in the written test will be invited for an interview.

LAST DATE FOR REGISTRATION IS **2nd July 2024.**

(Dr. Nisha Singh)
Training and Placement Officer
CCGPC, GGSIP University

JOB DESCRIPTION

Role 1: Analog Circuit Design

As an Analog Circuit Design Engineer, you will be involved in the design, development, testing, and troubleshooting of analog circuits such as amplifier, ADC, LDO etc on Finfet technologies. You will work closely with senior engineers and cross-functional teams to deliver high-performance and reliable solutions.

Key Responsibilities:

- Design and develop analog circuits for various applications, such as IoT, High speed design, bio-medical including power management, and communication systems.
- Conduct simulations and analysis of analog circuits to ensure performance and reliability.
- Perform testing and characterization of analog circuits and systems.

Role 2: Analog Layout Design

As an Analog Layout Design Engineer, you will be responsible for the layoutdesign ofanalog integrated circuits (ICs) such as amplifie, LDO, BGR, PLL etc. You will work closely with design engineers to ensure that the layouts meet performance, area, and power requirements.

Key Responsibilities:

- Design and implement layout solutions for analog integrated circuits (ICs) using both FinFET (e.g., 7nm technology) and planar technologies, based on schematic inputs.
- Ensure layout designs meet design specifications, including performance, area, and power constraints.
- Perform layout verification and validation using tools such as DRC (Design Rule Check), LVS (Layout vs. Schematic), and ERC (Electrical Rule Check).
- Collaborate with circuit design engineers to optimize layout for performance and manufacturability.
- Assist in the debugging and troubleshooting of layout-related issues.

Role 3: Digital circuit Design

As an Analog Layout Design Engineer, you will be responsible for the design and characterization of digital circuit such as Std. Cell library, Level shifter etc. You will work closely with senior engineers and cross-functional teams to deliver high-performance and reliable solutions.

Key Responsibilities:

- **Design and Development:** Assist in the design and development of digital circuits and systems, including logic gates, flip-flops, multiplexers, and other fundamental digital components.
- **Schematic Capture:** Create and modify schematics based on design specifications and project requirements.
- **Simulation and Testing:** Perform simulations to verify the functionality and performance of digital circuits. Conduct testing and debugging to identify and resolve issues.
- **Characterization of Digital circuit:**Analyze and characterize the performance of digital circuits under various conditions to ensure they meet design specifications and reliability standards.